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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/313,424	05/17/99	HUTTNER T	GR-98-P-8041

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EXAMINER	
KEBEDE, B	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 09/26/00

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/313,424	HUTTNER ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

1)☒ Responsive to communication(s) filed on *03 April 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) *1-6* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

a)☒ All b)☐ Some * c)☐ None of the CERTIFIED copies of the priority documents have been:

1.☒ received.

2.☐ received in Application No. (Series Code / Serial Number) _____ .

3.☐ received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. & 119(e).

Attachment(s)

15) ☒ Notice of References Cited (PTO-892)
16) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *7,8* .
18) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
19) ☐ Notice of Informal Patent Application (PTO-152)
20) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicants' election **without traverse** of Claims 7-15 in Paper No. 11 is acknowledged.

2. Claims 1-6 are withdrawn from further consideration.

Priority

3. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

4. The information disclosure statement filed on September 7, 2000 of Paper No.7 fails to comply with 37 CFR 1.98(a)(3) because it does not include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information, of each patent listed that is not in the English language. It has been placed in the application file, but the information referred to therein has not been considered.

Drawings

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, "providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates;

joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer " as recited in claim 10 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Claim Objections

6. Claims 7-15 are objected to as being improperly dependent of non-elected base independent base claim.

The dependency of claim 7 on the non-elected claim, claim 1, is improper.

Claims 8-15 are also objected as being dependent of the objected base claim.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 7-15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Although an attempt has been made to identify all instances of claim language non-complacence, such identification is extremely burdensome due to the large number of instances. Examples are provided herein below. Since such noncompliance confuses the claims to the extent that not all of the problems are ready apparent, then upon amendment, if an alternative interpretation of claim language requires a change in the rejection, the new rejection may properly **made final**.

Re claims 7, 13 and 14 the limitation "introducing the passivating substance X into one of the insulation layer and the monocrystalline silicon layer" in lines 5-6, 2-4 and 2-4 respectively is not clear to the Examiner whether applicants trying to claim between one of the two insulating layer or between the insulating layer and the mono-crystalline silicon layer. Therefore, the claim is vague and indefinite.

Claim 7 recites the limitation "the semiconductor substrate" in line 1. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the base layer" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the insulation layer" in lines 3-4. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the monocrystalline silicon layer " in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim 7 recites the limitation "the passivating substance X" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim 12 recites the limitation "the underlying insulation layer" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claims 8-15 are rejected as being dependent of the rejected base claim.

10. Applicants' cooperation is requested in reviewing the claims structure to ensure proper claim construction and to correct any subsequently discovered instances of claim language noncompliance. See *Morton International Inc.*, 28USPQ2d 1190, 1195 (CAFC, 1993).

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 7-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kadosh et al. (USPAT/5,893,739).

Re claim 7, Kadosh et al. teach a method of fabricating the semiconductor configuration comprising: providing a semiconductor structure having a base layer (10), an insulation layer (12), and a polycrystalline silicon layer (i.e. formed by the same material to form mono-crystalline silicon) (14) introducing a passivating substance X (not labeled) into one of the insulation layer (12) and the polycrystalline silicon layer (i.e. formed by the same material to form mono-crystalline silicon) (14) during or after the fabrication of the semiconductor structure (not labeled); and heat-treating the semiconductor structure with the passivating substance X (see Fig. 1a).

Re claim 8, as applied to claim 7 above, Kadosh et al. teach all the claimed limitations including the limitation of ion-implanting the passivating substance X (see Fig. 1a).

Re claim 9, as applied to claim 8 above, Kadosh et al. teach all the claimed limitations including the limitation of defining an implantation maximum for the passivating substance X in vicinity of an interface between the insulation layer and the polycrystalline (mono-crystalline) silicon layer (see Fig. 1c).

Re claim 11, as applied to claim 7 above, Kadosh et al. teach all the claimed limitations including the limitation of forming a covering oxide layer on the polycrystalline (mono-crystalline) silicon layer (see Fig. 1d).

Re claim 12, as applied to claim 7 above, Kadosh et al. teach all the claimed limitations including the limitation of patterning the polysilicon (mono-crystalline) silicon layer by etching away regions thereof down to the underlying insulation layer (see Figs. 1a and 2a).

Re claim 13, as applied to claim 12 above, Kadosh et al. teach all the claimed limitations including the limitation of patterning step is performed before the step of introducing the passivating substance X into one of the insulation layer and the polycrystalline (mono-crystalline) silicon layer (see Fig. 1g).

Re claim 14, as applied to claim 12 above, Kadosh et al. teach all the claimed limitations including the limitation of patterning step is performed after the step of introducing the passivating substance X into one of the insulation layer and the polycrystalline (mono-crystalline) silicon layer (see Figs. 1a and 2a).

Re claim 15, as applied to claim 7 above, Kadosh et al. teach all the claimed limitations including the limitation of doping the polycrystalline (mono-crystalline) silicon layer differently region by region by means of ion implantation; and performing the doping step after the step of introducing the passivating substance X and the heat-treating step (see Figs. 1a, 2a and 3a).

13. Claim10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kadosh et al. (USPAT/5,893,739) as applied to claim 7 above, in view of Sato et al. (USPAT/5,854.

Re claim 10, as applied to claim 7 above, Kadosh et al. teach all the claimed limitations including the limitation. Although, the limitations of providing two silicon semiconductor

substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer is well-known in the art Kadosh et al. do not disclose the claimed limitations. Sato et al. disclose providing two silicon semiconductor substrates; oxidizing and forming a respective oxide layer on the two silicon semiconductor substrates; selecting an introducing step from the group consisting of introducing the passivating substance X into at least one of the oxide layers, introducing the passivating substance X before the oxidation step into one of the silicon semiconductor substrates, and introducing the passivating substance X after the oxidation step into one of the silicon semiconductor substrates; joining the two silicon semiconductor substrates by contacting the two oxide layers; and partially removing one of the silicon semiconductor substrates and forming the monocrystalline silicon layer in order to form SOI (see Figs. 2A-2D).

Sato et al. suggest that "formation of mono-crystalline Si semiconductor layer on an insulator is well known as silicon-on-insulator (SOI) technique. Many investigations have been made thereon since the devices made by the SOI technique have many advantages which are not achievable with a bulk Si substrate for usual Si integrated circuits. The advantages brought about by the SOI technique are as below: 1. Ease of dielectric separation, and practicability of high integration, 2. High resistance against radioactive rays, 3. Low floating capacity, and

practicability of high speed operation, 4. Practicability of omission of a welling step, 5. Practicability of prevention of latching-up, 6. Practicability of thin film formation for complete depletion type field effect transistor, and so forth." (see Sato et al. Col. 3, lines 42-59) One of ordinary skill in the art would have motivated to use SOI technique as Sato et al. disclosed in order to improve the overall device performance and applicability of the device.

Therefore, it would have been obvious to one having ordinary skill in the art at the time of applicant(s) claimed invention was made to have provided , Kadosh et al. reference with SOI technique as taught by Sato et al. because the device performance would have been improved.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure Shiratake et al. (USPAT/5,801,427), Gardner et al. (USPAT/6,020,232), Shigyo et al. (USPAT/6,051,452) also disclose similar inventive subject matter.

Correspondence

15. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (703) 306-4511. The examiner can normally be reached on 8-5 Monday to Friday.

16. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (703) 308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

17. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Brook Kebede
BK
September 21, 2000

Trung Dang
Primary Examiner